

10  
FOR ( i=0; i<2; i=i+1)  
11 { begin  
out [ i ] = 8 ' b10101010;  
enable [ i ] = up [ 2 \* i ];  
end }

**Figure 1**

(Prior Art)

reg y [3:0];  
13 WHILE ( x <= y )  
12 begin  
fpl\_bit [ x + y ] - mm\_iru [ x - y ];  
end

**Figure 2**

(Prior Art)

16  
18  
20  
14  
22  
FOR ( INIT; EXIT; INC )  
begin  
BODY\_OF\_STATEMENTS;  
end

**Figure 3**

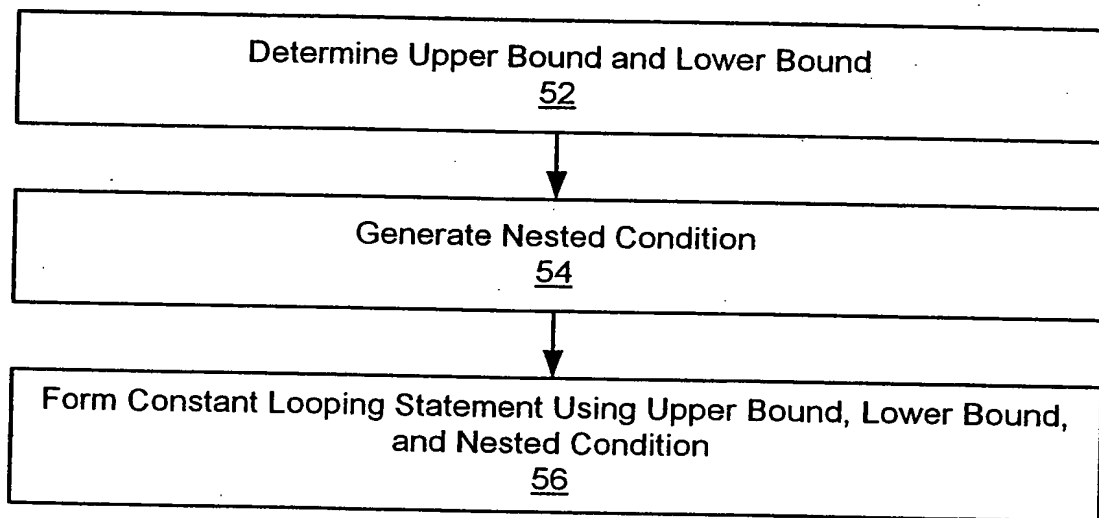
(Prior Art)

2/3

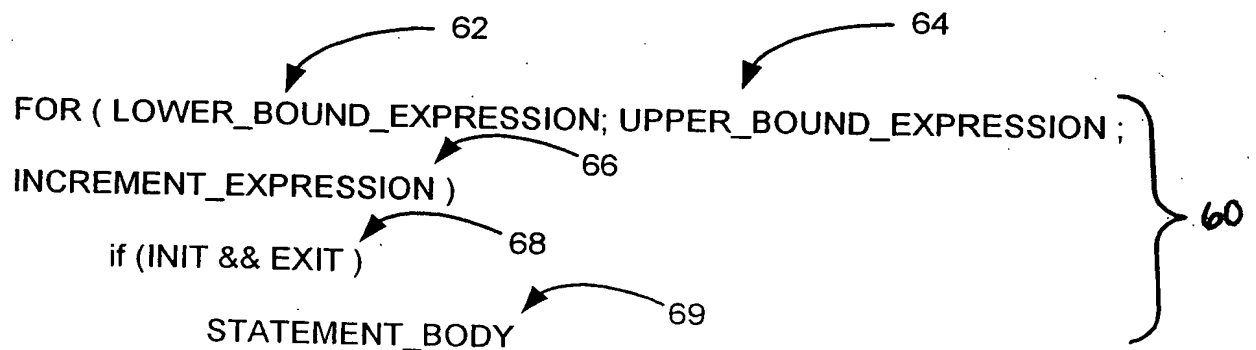
```
out [ 0 ] = 8 ' b10101010 ;  
enable [ 0 ] = ~up [ 0 ] ;  
  
out [ 0 ] = 8 ' b10101010 ;  
enable [ 0 ] = ~up [ 2 ] ;
```

} 24

**Figure 4**



**Figure 5**



**Figure 6**